CLAIM AMENDMENTS

Claim Amendment Summary

Claims pending

- At time of the Action: Claims 1-58.
- After this Response: Claims 1-10, 12-25, 27-37, 39-40, 46-54, and 56-58.

Canceled or Withdrawn Claims: 11, 26, 38, 41-45, and 55.

Amended Claims: 1, 12, 13, 17, 42, 46, and 56.

CLAIM LISTING:

1. **(Currently Amended)** An apparatus, comprising: a multiprocessor system that uses cache coherency for accessing memory; and a maintenance interface unit integrated within the multiprocessor system configured to (i) provide a backdoor access to the multiprocessor system on-behalf of a peripheral maintenance system and (ii) perform operations within the multiprocessor system while participating in the cache coherency wherein at least one of the operations performed by the maintenance interface unit includes handling a rogue message.

2. **(Original)** The apparatus as recited in claim 1, wherein the apparatus includes one or more chips.

3. **(Original)** The apparatus as recited in claim 1, wherein the backdoor interface is integrated on a chip comprising part of the multiprocessor system, and the peripheral maintenance system is coupled to the multiprocessor system via the backdoor interface, but is not integrated on the same chip as the backdoor interface.

4. **(Original)** The apparatus as recited in claim 1, wherein the maintenance interface unit is further configured to permit the peripheral maintenance processor to read and/or write to memory while maintaining cache coherency.

5. **(Original)** The apparatus as recited in claim 1, wherein the maintenance interface unit is further configured to permit the peripheral maintenance processor to communicate with one or more operating systems functioning in the multiprocessor system.

6. **(Original)** The apparatus as recited in claim 1, wherein the maintenance interface unit is further configured to permit the peripheral maintenance processor to initialize the multiprocessor system.

7. **(Original)** The apparatus as recited in claim 1, wherein the maintenance interface unit is further configured to automatically notify the peripheral maintenance processor if an error condition is detected in the multiprocessor system.

8. **(Original)** The apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit includes recognizing when a

device and/or operating system is not available and automatically notifying the multiprocessor system of the unavailability.

9. **(Original)** The apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit includes recognizing when a device and/or operating system is not available, automatically notifying the multiprocessor system of the unavailability, and automatically notifying the peripheral maintenance processor of the unavailability.

10. **(Original)** The apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit includes issuing an interruption command to the multiprocessor system.

11. **(Canceled)**.

12. **(Currently Amended)** ~~The apparatus as recited in claim 1,~~ An apparatus, comprising: a multiprocessor system that uses cache coherency for accessing memory; and a maintenance interface unit integrated within the multiprocessor system configured to (i) provide a backdoor access to the multiprocessor system on-behalf of a peripheral maintenance system and (ii) perform operations within the multiprocessor system while participating in the cache coherency, wherein at least one of the operations performed by the maintenance interface unit includes receiving a rogue message and automatically responding to an entity within the multiprocessor system that generated the rogue message.

13. (**Currently Amended**) ~~The apparatus as recited in claim 1,~~ An apparatus, comprising: a multiprocessor system that uses cache coherency for accessing memory; and a maintenance interface unit integrated within the multiprocessor system configured to (i) provide a backdoor access to the multiprocessor system on-behalf of a peripheral maintenance system and (ii) perform operations within the multiprocessor system while participating in the cache coherency, wherein at least one of the operations performed by the maintenance interface unit includes receiving a rogue message and automatically notifying the peripheral maintenance processor of the rogue message.

14. **(Original)** The apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit includes performing error testing.

15. **(Original)** The apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit includes injecting an error condition into the multiprocessor system.

16. **(Original)** The apparatus as recited in claim 1, wherein at least one of the operations performed by the maintenance interface unit includes injecting a plurality of artificial requests into the multiprocessor system to enable the peripheral maintenance processor to monitor performance of the multiprocessor system.

17. **(Currently Amended)** A system, comprising: a multiprocessor system that uses cache coherency for accessing memory; a peripheral maintenance system,

configured to monitor performance of the multiprocessor system and service the multiprocessor system if aberrations are detected with the performance; and a maintenance interface unit integrated within the multiprocessor system, configured to provide backdoor accessibility to the multiprocessor system on-behalf of the peripheral maintenance system, and perform operations within the multiprocessor system while participating in the cache coherency, wherein at least one of the operations performed by the maintenance interface unit includes handling a rogue message.

18. **(Original)** The system as recited in claim 17, wherein the peripheral maintenance system is coupled to the multiprocessor system via the backdoor interface and is not integrated within the multiprocessor system.

19. **(Original)** The system as recited in claim 17, wherein the maintenance interface unit is further configured to permit the peripheral maintenance processor to read and/or write to memory while maintaining cache coherency.

20. **(Original)** The system as recited in claim 17, wherein the maintenance interface unit is further configured to permit the peripheral maintenance processor to communicate with one or more operating systems functioning in the multiprocessor system.

21. **(Original)** The system as recited in claim 17, wherein the maintenance interface unit is further configured to permit the peripheral maintenance processor to initialize the multiprocessor system.

22. **(Original)** The system as recited in claim 17, wherein the maintenance interface unit is further configured to automatically notify the peripheral maintenance processor if an error condition is detected in the multiprocessor system.

23. **(Original)** The system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes recognizing when a device and/or operating system is not available and automatically notifying the multiprocessor system of the unavailability.

24. **(Original)** The system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes recognizing when a device and/or operating system is not available, automatically notifying the multiprocessor system of the unavailability, and automatically notifying the peripheral maintenance processor of the unavailability.

25. **(Original)** The system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes issuing an interruption command to the multiprocessor system.

26. **(Canceled).**

27. **(Original)** The system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes receiving a rogue

message and automatically responding to an entity within the multiprocessor system that generated the rogue message.

28. **(Original)** The system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes receiving a rogue message and automatically notifying the peripheral maintenance processor of the rogue message.

29. **(Original)** The system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes performing error testing.

30. **(Original)** The system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes injecting an error condition into the multiprocessor system.

31. **(Original)** The system as recited in claim 17, wherein at least one of the operations performed by the maintenance interface unit includes injecting a plurality of artificial requests into the multiprocessor system to enable the peripheral maintenance processor to monitor performance of the multiprocessor system.

32. **(Currently Amended)** In a multiprocessor system that uses cache coherency for accessing memory, a method comprising: providing a backdoor access to the multiprocessor system on-behalf of a peripheral maintenance system, the backdoor access integrated within the multiprocessor system in the form of a maintenance interface unit; ~~and~~

treating the maintenance interface unit as one of the processors in the multiprocessor system to enable participation in the cache coherency; logging a rogue message automatically; and notifying the peripheral maintenance processor of the rogue message automatically.

33. **(Original)** The method as recited in claim 32, where treating the maintenance interface unit as one of the processor in the multiprocessor system further permits the maintenance interface unit to (i) communicate with, (ii) issue commands to, and (iii) monitor other devices and systems integrated within the multiprocessor system while participating in the cache coherency without having to interrupt the multiprocessor system.

34. **(Original)** The method as recited in claim 32, wherein providing the backdoor access and treating the maintenance interface unit as one of the processors in the multiprocessor system further permits the peripheral maintenance system to read, write, and initialize memory via the maintenance interface unit while participating in the cache coherency.

35. **(Original)** The method as recited in claim 32, wherein providing the backdoor access comprises: receiving an indication at the maintenance interface unit that a particular entity within the multiprocessor system is unavailable; notifying the multiprocessor system and the peripheral maintenance system of the unavailable entity; and responding to any messages sent to the unavailable entity after receipt of the indication automatically.

36. **(Original)** The method as recited in claim 32, wherein providing the backdoor access comprises permitting the peripheral maintenance processor to communicate with one or more operating systems functioning in the multiprocessor system.

37. **(Original)** The method as recited in claim 32, wherein providing the backdoor access comprises automatically notifying the peripheral maintenance processor if an error condition is detected in the multiprocessor system.

38. **(Cancelled)**

39. **(Original)** The method as recited in claim 32, wherein the providing the backdoor access comprises injecting an error condition into the multiprocessor system.

40. **(Original)** The method as recited in claim 32, further comprising injecting a plurality of artificial requests into the multiprocessor system via the maintenance interface unit.

Claims 41-45 (Cancelled).

46. **(Currently Amended)** Integrated within a cache-coherent multiprocessor system, a maintenance interface unit, comprising: a transaction unit, configured to provide a backdoor access for a peripheral maintenance system to the multiprocessor system and perform tasks on-behalf of a peripheral maintenance system in the multiprocessor system while participating in cache coherency of the multiprocessor system without having to interrupt the multiprocessor system, wherein the peripheral maintenance system is not integrated within the multiprocessor system; and a housekeeping module configured to

perform housekeeping operations in the multiprocessor system automatically, wherein the housekeeping module comprises a rogue message module configured to receive a rogue message and automatically respond to an entity within the multiprocessor system that generated the rogue message.

47. **(Original)** The maintenance interface unit as recited in claim 46, further comprising an off-chip interface coupled to the peripheral maintenance system, configured to provide a communication link between the peripheral maintenance system and the maintenance interface unit.

48. **(Original)** The maintenance interface unit as recited in claim 46, further comprising an on-chip interface configured to provide a communication link between the maintenance interface unit and components integrated in the multiprocessor system.

49. **(Original)** The maintenance interface unit as recited in claim 46, wherein the transaction unit comprises a read/write module configured to permit the peripheral maintenance processor to read and/or write to memory while maintaining cache coherency.

50. **(Original)** The maintenance interface unit as recited in claim 46, wherein the transaction unit comprises an operating system module configured to permit the peripheral maintenance processor to communicate with one or more operating systems functioning in the multiprocessor system.

51. **(Original)** The maintenance interface unit as recited in claim 46, wherein the transaction unit comprises an initialization module, configured to permit the peripheral maintenance processor to initialize the multiprocessor system.

52. **(Original)** The maintenance interface unit as recited in claim 46, wherein the housekeeping module comprises an error report module configured to automatically notify the peripheral maintenance processor if an error condition is detected in the multiprocessor system.

53. **(Original)** The maintenance interface unit as recited in claim 46, wherein the housekeeping module comprises a device notification module configured to recognize when a device and/or operating system is not available and automatically notify the multiprocessor system of the unavailability.

54. **(Original)** The maintenance interface unit as recited in claim 46, wherein the housekeeping module comprises a device notification module configured to recognize when a device and/or operating system is not available, automatically notify the multiprocessor system of the unavailability, and automatically notify the peripheral maintenance processor of the unavailability.

55. **(Cancelled)**.

56. **(Currently Amended)** ~~The maintenance interface unit as recited in claim 46~~ Integrated within a cache-coherent multiprocessor system, a maintenance interface unit,

comprising: a transaction unit, configured to provide a backdoor access for a peripheral maintenance system to the multiprocessor system and perform tasks on-behalf of a peripheral maintenance system in the multiprocessor system while participating in cache coherency of the multiprocessor system without having to interrupt the multiprocessor system, wherein the peripheral maintenance system is not integrated within the multiprocessor system; and a housekeeping module configured to perform housekeeping operations in the multiprocessor system automatically, wherein the housekeeping module comprises a rogue message module configured to receive a rogue message, respond automatically to an entity within the multiprocessor system that generated the rogue message, and notify automatically the peripheral maintenance processor of the rogue message.

57. **(Original)** The maintenance interface unit as recited in claim 46, wherein the transaction unit comprises an error generation module, configured to issue artificial error messages within the multiprocessor system to enable the peripheral maintenance system to perform error testing.

58. **(Original)** The maintenance interface unit as recited in claim 46, wherein the transaction unit comprises an injection module, configured to inject a plurality of artificial requests into the multiprocessor system to enable the peripheral maintenance processor to monitor performance of the multiprocessor system.